

IN THE CLAIMS

Please amend the claims to the following.

- 1 1. (Currently Amended) A system for maintaining cache coherency in a CMP
2 comprising:
3 an integrated circuit including
4 one or more processor cores, wherein the one or more processor cores
5 each include a private cache;
6 a shared cache separate from the plurality of cores to be shared by the one
7 or more processor cores; and
8 a ring to connect the one or more processor cores and the shared cache.
- 1 2. (Canceled)
- 1 3. (Previously Amended) The system of claim 1 wherein the shared cache
2 includes one or more banks.
- 1 4. (Original) The system of claim 3 wherein the one or more cache banks is
2 responsible for a subset of a physical address space of the system.
- 1 5. (Original) The system of claim 1 wherein the one or more processor cores are
2 write-thru.
- 1 6. (Original) The system of claim 5 wherein the one or more processor cores writes
2 data through to the shared cache.

- 1 7. (Original) The system of claim 1 wherein the one or more processor cores
2 includes a merge buffer.
- 1 8. (Original) The system of claim 7 wherein data is stored in the merge buffer.
- 1 9. (Original) The system of claim 8 wherein the merger buffer purges data to the
2 shared cache.
- 1 10. (Original) The system of claim 1 wherein the one or more processor cores
2 accesses data from the shared cache.
- 1 11. (Original) The system of claim 8 wherein the merger buffer coalesces multiple
2 stores to a same block.
- 1 12. (Original) The system of claim 1 wherein the ring is a synchronous, unbuffered
2 bidirectional ring interconnect.
- 1 13. (Original) The system of claim 12 wherein a message has a fixed deterministic
2 latency around the ring interconnect.

- 1 14. (Currently Amended) An apparatus comprising:
2 an integrated circuit including: a plurality of cores and a shared memory
3 connected in a ring, the shared cache being separate from the plurality of
4 cores, wherein each of the plurality of cores includes a private cache
5 memory, and wherein the shared memory is accessible by each of the
6 plurality of cores.
- 1 15. (Previously Added) The apparatus of claim 14, wherein the plurality of cores
2 and the shared memory are connected in a ring with a synchronous unbuffered bi-
3 directional ring interconnect.
- 1 16. (Previously Added) The apparatus of claim 14, wherein the shared memory is a
2 shared cache including a plurality of blocks, and wherein the shared cache is
3 capable of holding each of the plurality of blocks in a cache coherency state.
- 1 17. (Previously Added) The apparatus of claim 16, wherein the cache coherency
2 state for each of the plurality of blocks is selected from a group consisting of (1) a
3 not present state, (2) a present and owned by a core of the plurality of cores state,
4 (3) a present, not owned, and custodian is a core of the plurality of cores state,
5 and (4) a present, not owned, and no custodian state.

1 18. (Currently Amended) An system comprising:
2 a processor including: a plurality of cores and a shared memory separately
3 coupled ~~together~~ with an unbuffered bi-directional ring interconnect,
4 wherein each of the plurality of cores is associated with a private cache
5 memory, and wherein the shared memory is accessible by each of the
6 plurality of cores; and
7 a system memory associated with the processor ~~die~~ to hold elements to be stored
8 by the shared memory.

1 19. (Previously Added) The apparatus of claim 18, wherein the shared memory is a
2 shared cache including a plurality of blocks, and wherein the shared cache is
3 capable of holding each of the plurality of blocks in a cache coherency state.

1 20. (Previously Added) The apparatus of claim 19, wherein the cache coherency
2 state for each of the plurality of blocks is selected from a group consisting of (1) a
3 not present state, (2) a present and owned by a core of the plurality of cores state,
4 (3) a present, not owned, and custodian is a core of the plurality of cores state,
5 and (4) a present, not owned, and no custodian state.